Amendments to the Specification:

Please replace paragraphs [0006], [0011], [0015], [0016], [0030], [0033], [0042], [0043], [0044], and [0072] respectively with the following rewritten paragraphs:

[0006] The converter is said to be non-isolated in the sense that it comprises ~~said~~ the first and second circuit branches respectively interconnecting ~~said~~ the first and second negative terminals and ~~said~~ the first and second positive terminals. Such a converter is contrasted with an isolated converter in which the first pair of terminals is isolated from the second pair of terminals.

[0011] According to some embodiments of a multicellular voltage converter has a fault mode of operation in which a determined cell can be taken out of service independently of the other cells when ~~said~~ the cell suffers a malfunction, while minimizing power consumption in normal operation.

[0015] n cells connected in parallel, where n is an integer greater than unity, disposed between said first positive and negative terminals and between ~~said~~ the second positive and negative terminals, each cell comprising a chopper DC/DC converter, each having a first circuit branch interconnecting ~~said~~ the first and second negative terminals, a second circuit branch including an inductor and interconnecting said first and second positive terminals, chopper means comprising at least one chopper switch, and a management unit adapted to control OFF and ON switching of the chopper switch with a determined duty ratio;

[0016] in which each cell further comprises a single protection transistor disposed in ~~said~~ the second circuit branch and associated with a protection management unit for taking said cell out of service independently of the other cells.

[0030] In the figures, in order to show clearly the orientation of the transistors used, the letters D and S designate respectively the drain ~~at~~ and the source of each transistor, in correspondence with the orientation specified in the description for that transistor.

[0033] In each of these individual converters 100, 200, . . . , 600, a capacitor 16, 26, . . . , 66, e.g. a 30 microfarad (.mu.F) capacitor, interconnects the terminals 1 and 2 in order to store on the 42 V network side the electric charge that is transferred by ~~said~~ the individual converter 100, 200, . . . , 600. Similarly, in each individual converter 100, 200, . . . , 600, another capacitor 17, 27, . . . , 57, e.g. likewise a 30 .mu.f capacitor, interconnects the terminals 3 and 4 in order to store, on the 14 V network side, the electric charge transferred by the individual converter 100, 200, . . . , 600. In operation, each of the two networks respectively at 42 V and at 14 V, consumes some of the electric charge in the respective sets of capacitors 16, 26, . . . , 66 and 17, 27, . . . , 67.

[0042] FIG. 2 shows the architecture for controlling the individual converter 100 of FIG. 1. It comprises a controller C1 whose inputs receive ~~said~~ the high voltage by wires 101 and 102 connected respectively to the terminals 1 and 2, said low voltage by wire 103 connected to the terminal 3, and the voltage across the terminals of the resistor 15 by wires 150 and 151. In a control mode using pulse width modulation and known to the person skilled in the art, the controller C1 controls the buck transistor 11 by OFF or ON signals transmitted to its grid by wire 110, with pulses being at a determined periodicity, e.g. corresponding to a frequency of 70 kilohertz (kHz).

[0043] A controller analogous to the controller C1 is connected in the same manner in each of the five other individual converters 200, . . . , 600 to perform an identical function in each of those circuits. Advantageously, the six controllers issue respective pulses at the same pulse periodicity, and are taken into consideration in a determined cyclical order, so that pulses from two successive individual converters in ~~said~~the order are offset by a shift equal to one-sixth of the period of the control pulses from each individual converter.

[0044] For the individual converter 100, a detector D1 has two inputs receiving the voltage between the drain and the source of the buck transistor 11 via, two wires 111 and 112. In normal operation of the individual converter 100, the detector D1 transmits a signal to a

protection management unit P so that it applies a certain voltage via wire 130 to the grid of the protection transistor 13, e.g. a voltage lying in the range 5 V to 10 V relative to the source of ~~said~~the protection transistor 13, so as to hold the protection transistor 13 in an ON or conductive state.

[0072] This position for the protection transistor 13, 23, . . . , 63 is preferred to a position situated between the buck transistor 11, 21, . . . , 61 and a node connecting the capacitor 16, 26, . . . , 66 to the terminal 1. The current flowing in the loop formed by the capacitor 16, 26, . . . , 66, the buck transistor 11, 21, . . . , 61, and the boost transistor 12, 22, . . . , 62 is a chopped current that is subject to sudden changes, so it is particularly advantageous to reduce the physical size of this loop in order to reduce disturbances due to any parasitic self-inductance in ~~said~~the loop, or indeed due to any radiation transmitted from ~~said~~the loop.